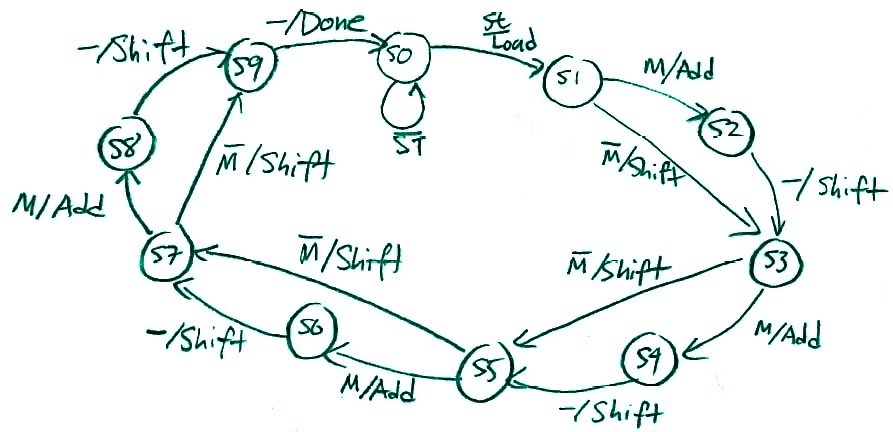
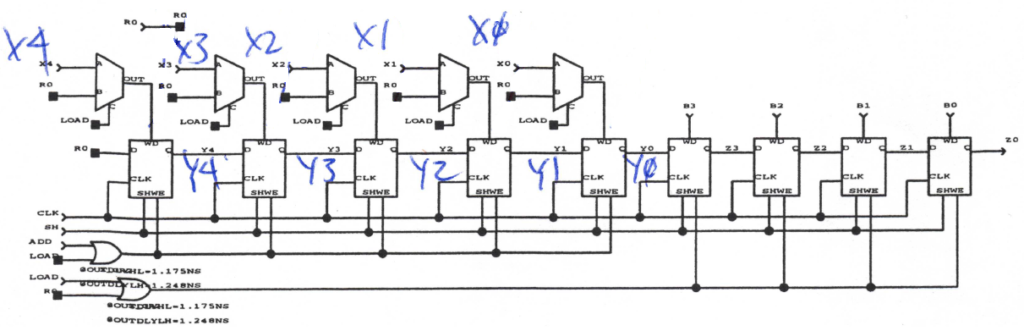
**Hw 3 – solution**

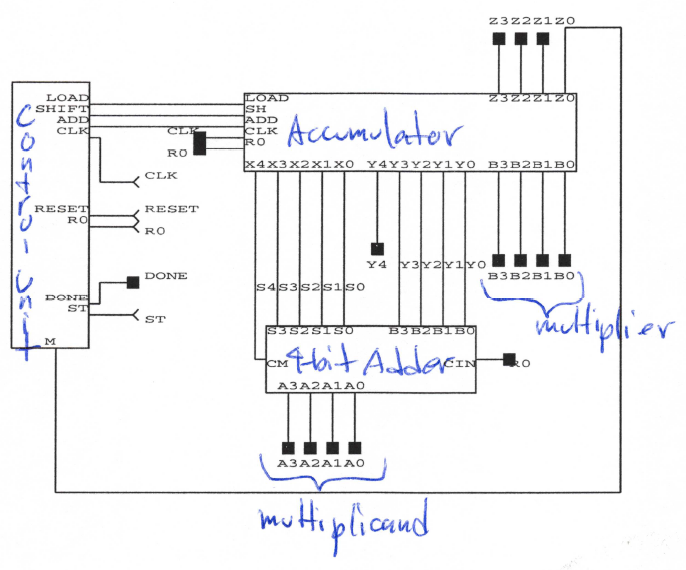
**Problem 1.** The solution for 4 x 4 array multiplier is given in text book pages 238 & 239

You need to extend it to 8 x 8 – as far as the ASM chart ,the following is a control diagram of the 4 bit array case again it can be extended to 8 bit array as well

Multiplication is performed by first loading the 4-bit multiplicand into the adder and loading the 4-bit multiplier into the lower 4 flip-flops of the register. The multiplier is shifted out of the register bit-by-bit and checked for a high bit. When the bit is high, the multiplicand is added to the shifted result stored within the register. The control unit sends shift and add signals to the accumulator depending on the value of the bits received from the multiplier. This shifting and adding behavior simulates the shifting and added performed in multiplying two binary numbers by hand.

The control unit is a 10 state Mealy state machine that configures add and shift signals based on the output from the accumulator. The state diagram is shown in Fig 1b. The control unit requires 4 D flip-flops to represent all the states. [](https://www.echopapers.com/wp-content/uploads/2017/01/img_587bf10df16f1.png)

[](https://www.echopapers.com/wp-content/uploads/2017/01/img_587bf24a4d54b.png)

[](https://www.echopapers.com/wp-content/uploads/2017/01/img_587c0bee30e18.png)

**Problem 2 :** BCD to binary conversion An example of this problem is given in our document section of canvas – the number is 857 you include it in register A which will be 12 bit long

bcd2 bcd1 bcd0 where bcd2 is 1000 bcd1 is 0101 and bcd0 is 0111

Make the register B a 12 bit wide to start with – and follow the instruction on the BCD to binary conversion document posted in out canvas site. Eventually the register B will be 10 bits wide. The for the state diagram please see the document on BCD to binary conversion in FPGA in our canvas site